TITLE

[0001] Monolithic Power Semiconductor Structures

CROSS-REFERENCE TO RELATED APPLICATIONS

[0002] This application claims the benefit of priority to U.S. Application Numbers 60/529,340 and 60/542,434, filed December 12, 2003 and February 5, 2004, respectively, the entire disclosures of which are hereby incorporated by reference as if set forth at length herein.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

[0003] Not applicable

REFERENCE OF A "MICROFICHE APPENDIX"

[0004] Not applicable

BACKGROUND OF THE INVENTION

1. Field of Invention

[0005] The present invention relates, in general, to semiconductors and, more particularly, to a novel monolithic semiconductor structure having one or more pairs of semiconductor devices combined on a semiconductor substrate.

2. Brief Description of the Prior Art

[0006] As the operating voltage of microprocessors approaches the one-volt mark, operating currents continue to increase. Today's high-end notebook computers consume 20A. Servers and high-end desktop computers presently require 60 to 90A. The next-generation GHz class of microprocessors will require current as high as 130A. These

changes in operating conditions challenge power components to maintain and monitor acceptable efficiency levels.

[0007] Power components may use isolated forward converters to maintain acceptable efficiency levels and reduce power dissipation. A common isolated forward converter topology for the computer, telecom and networking industry has one discrete vertical planar or trench MOSFET on the primary side and two discrete vertical planar or trench MOSFETs on the secondary side as synchronous rectifiers.

[0008] FIG. 1A-B depict aspects of prior art synchronous rectifier circuits. Specifically, FIG. 1A is a schematic of a prior art self-driven synchronous rectifier using three discrete trench MOSFETs, M1, M2 and M3. Alternatively, FIG. 1B is a schematic diagram of an external-driven synchronous rectifier using three discrete trench MOSFETs, M1, M2 and M3. In both topologies, M1 functions as a primary-side control switch, M2 functions as a secondary-side synchronous forward and M3 functions as a secondary-side synchronous catch.

[0009] International Rectifier's 30V-rated IRF7822 or IRF6603 (DirectFETTM) products are examples of widely used devices using discrete vertical planar or trench MOSFETs in rectification applications.

[0010] Power components may also use two discrete vertical planar or trench MOSFETs to monitor operating conditions - one vertical planar or trench MOSFET functions as a main switch with its current monitored by a second ("external") vertical planar or trench MOSFET which functions as a sense. FIG. 2 is a schematic diagram illustrating the foregoing prior art configuration. As shown, the source and gate terminals of the power MOSFET switch are connected to the corresponding source and gate terminals of the

external MOSFET sense. The drain terminal of the external MOSFET sense monitors the voltage or current at the drain of the MOSFET switch.

[0011] Both low device on-resistance and low gate charge are necessary to run high-frequency forward converters or increase power density in the same form-factor. Vertical planar or trench MOSFETs exhibit very low on-resistance but have a high gate charge due to the inherent vertical device structures.

[0012] Moreover to greatly reduce parts count, PCB space, and interconnect parasitics, it is desirable to combine secondary side MOSFETs or switch and sense MOSFETs on a single substrate However, because vertical planar and trench MOSFETs have a common backside drain terminal, it is very complicated and expensive to combine two vertical planar or trench MOSFETs on a single semiconductor substrate.

[0013] On the other hand, lateral power MOSFETs, that until now are exclusively used in power ICs and as discrete RF devices, offer very low gate charge and reasonably low on-resistance. However, the use of lateral power MOSFETs is limited to small chip sizes and current ratings due to high metal interconnect parasitic resistance.

SUMMARY OF THE INVENTION

[0014] The present invention addresses the aforementioned limitations of the prior art by providing, in accordance with one aspect of the present invention, a monolithic semiconductor structure or device having at least two lateral power transistor devices combined on a single semiconductor substrate.

[0015] In accordance with a second aspect of the present invention, there is provided a monolithic self-driven synchronous rectifier structure comprising a pair of lateral power MOSFETs combined on a single semiconductor substrate.

[0016] In accordance with a third aspect of the present invention, there is a provided a monolithic external-driven synchronous rectifier structure comprising a pair of lateral power MOSFETs combined on a single semiconductor substrate.

[0017] In accordance with additional aspects of the present invention, there is provided exemplary embodiments of monolithic structures having an integrated drain sense and comprising at least two lateral power MOSFETs combined on a single semiconductor substrate.

[0018] These and other aspects, features and advantages of the present invention will become better understood with regard to the following description, appended claims, and accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] Exemplary embodiments of the present invention are now briefly described with reference to the following drawings:

[0020] FIG. 1 depicts one aspect of the prior art in accordance with the teachings presented herein.

[0021] FIG. 2 depicts a second aspect of the prior art in accordance with the teachings presented herein.

[0022] FIG. 3 depicts an aspect of the present invention in accordance with the teachings presented herein.

[0023] FIG. 4 depicts a second aspect of the present invention in accordance with the teachings presented herein.

[0024] FIG. 5 depicts a third aspect of the present invention in accordance with the teachings presented herein.

[0025] FIG. 6 depicts a fourth aspect of the present invention in accordance with the teachings presented herein.

[0026] FIG. 7 depicts a fifth aspect of the present invention in accordance with the teachings presented herein.

[0027] FIG. 8 depicts a sixth aspect of the present invention in accordance with the teachings presented herein.

[0028] FIG. 9 depicts a second aspect of the present invention in accordance with the teachings presented herein.

[0029] FIG. 10 depicts an eighth aspect of the present invention in accordance with the teachings presented herein.

[0030] FIG. 11 depicts a ninth aspect of the present invention in accordance with the teachings presented herein.

DESCRIPTION OF THE INVENTION

[0031] The aspects, features and advantages of the present invention will become better understood with regard to the following description with reference to the accompanying drawings. What follows are preferred embodiments of the present invention. It should be apparent to those skilled in the art that the foregoing is illustrative only and not limiting, having been presented by way of example only. All the features disclosed in this description may be replaced by alternative features serving the same purpose, and equivalents or similar purpose, unless expressly stated otherwise. Therefore, numerous other embodiments of the modifications thereof are contemplated as falling within the scope of the present invention as defined herein and equivalents thereto.

[0032] Because of the common backside drain terminal, current vertical planar and trench power MOSFET devices are very difficult and expensive to combine on a single semiconductor substrate to create a monolithic semiconductor structure. However, provided herein are exemplary embodiments of novel monolithic semiconductor structures having at least one first lateral semiconductor device combined with at least one second lateral semiconductor device on a single semiconductor substrate. Each of the lateral semiconductor devices is constructed such that source, drain and gate terminals terminate on the top surface of the device. A suitable example of such a lateral semiconductor device is a conventional lateral power MOSFET. Another suitable example, is a novel power semiconductor device described in Applicant's International Application No. PCT/US2003/031603, entitled "Power MOSFET," the disclosure of which is incorporated by reference in its entirety herein. The monolithic structures provided herein are fabricated by conventional methods.

[0033] MONOLITHIC SYNCHRONOUS RECTIFIERS

[0034] FIGURE 3

[0035] FIG. 3A is a schematic diagram of an exemplary embodiment of a monolithic semiconductor structure 300 constructed in accordance with the present invention that is suitable for use as a self-driven synchronous rectifier. The monolithic structure 300 has three leads and comprises a pair of lateral power MOSFETs 102 and 104, which are combined on a single semiconductor substrate 106. The monolithic structure 300 has three leads - common source terminal (CS) 108 and two electrically isolated drain terminals (D1 & D2) 109 and 110. The gate terminals (not shown) are connected internally.

[0036] The source terminal of the MOSFET 102 is connected to the source terminal of the MOSFET 104 to function as the common source terminal (CS) 108 of the structure 300. The drain terminal of the MOSFET 102 functions as the isolated drain terminal (D1) 109 of the structure 300 and is also connected to the gate terminal 113 of the MOSFET 104. The drain terminal of the MOSFET 104 functions as the isolated drain terminal (D2) 110 of the structure 300 and is also is connected to the gate terminal 112 of the MOSFET 102.

[0037] FIG. 3B is a schematic diagram of an exemplary embodiment of a monolithic semiconductor structure 500 constructed in accordance with the present invention that is suitable for use as an external-driven synchronous rectifier. The monolithic structure 500 has five leads and comprises a pair of lateral power MOSFETs 102 and 104, which are combined on a single semiconductor substrate 106. The monolithic structure 500 has five leads - common source terminal (CS) 108, two electrically isolated drain terminals (D1 & D2) 109 and 110 and two electrically isolated gate terminals (G1 & G2) 112 and 113.

[0038] The source terminal of the MOSFET 102 is connected to the source terminal of the MOSFET 104 to function as the common source terminal (CS) 108 of the structure 500. The drain terminal of the MOSFET 102 functions as the isolated drain terminal (D1) 109 of the structure 500 and the drain terminal of the MOSFET 104 functions as the isolated drain terminal (D2) 110 of the structure 500. The gate terminal of the MOSFET 102 functions as the isolated gate terminal (G1) 112 of the structure 500 and the gate terminal of the MOSFET 104 functions as the isolated drain terminal (G2) 113 of the structure 500.

[0039] FIGURE 4

[0040] FIG 4A is an exemplary, physical cross-sectional diagram of a monolithic structure 302, which implements the schematic shown in FIG. 3A. FIG. 4A also depicts a schematic diagram of the leads interconnecting the drain and source terminals of the structure 302. The gate terminals (not shown) are connected internally. The monolithic structure 302 shows four pairs of lateral power MOSFETs (eight individual MOSFETs), which are combined on the semiconductor substrate 106. The underlying transistors of the eight lateral power MOSFETs are interleaved to create the alternating D1-D2 pattern shown in FIG. 4A. The monolithic structure 302 has three leads - common source CS and isolated drains, D1 and D2.

[0041] FIG. 4B is an exemplary, physical cross-sectional diagram of a monolithic structure 502, which implements the schematic shown in FIG. 3B. FIG. 4B also illustrates a schematic diagram of the leads interconnecting the drain, source and gate terminals of the structure 502. The monolithic structure 502 shows four pairs of lateral power MOSFETs (eight individual MOSFETs), which are combined on the semiconductor substrate 106. The underlying transistors of the eight lateral power MOSFETs are interleaved to create the alternating pattern shown in FIG. 4B. The monolithic structure 502 has five leads, common source CS, isolated drains, D1 and D2 and isolated gate terminals G1 & G2.

[0042] FIGURE 5

[0043] FIG. 5A is an exemplary, physical cross-sectional diagram of an alternative monolithic structure 304, which implements the schematic shown in FIG. 3A. FIG. 5A also depicts a schematic diagram of the leads interconnecting the drain and source terminals of the structure 304. The gate terminals (not shown) are connected internally.

As shown, the monolithic structure 304 has four pairs of lateral power MOSFETs (eight individual MOSFETs), which are combined on a single semiconductor substrate 106 having two separate cell sections: D1/CS section and D2/CS section. Each of the cell sections D1/CS and D2/CS includes two pairs of MOSFETs. The underlying transistors of the MOSFETs are connected in parallel to create the pattern shown in FIG. 5A. The monolithic structure 304 has three leads - common source CS and isolated drains, D1 and D2.

[0044] FIG. 5B is an exemplary, physical cross-sectional diagram of an alternative monolithic structure 504, which implements the schematic shown in FIG. 3B. FIG. 5B also depicts a schematic diagram of the leads interconnecting the drain and source terminals of the structure 504. As shown, the monolithic structure 504 has four pairs of lateral power MOSFETs (eight individual MOSFETs), which are combined on a single semiconductor substrate 106 having two separate cell sections: D1/CS and D2/CS. Each of the cell sections, D1/CS and D2/CS, includes two pairs of MOSFETs. The underlying transistors of the MOSFETs are connected in parallel to create the pattern shown in FIG. 5B. The monolithic structure 504 has five leads - common source CS, isolated drains, D1 and D2 and isolated gate terminals G1 & G2.

[0045] MONOLITHIC STRUCTURES HAVING AN INTEGRATED DRAIN SENSE

[0046] FIG. 6 is a schematic diagram of an exemplary embodiment of a monolithic structure 600 having an integrated drain sense that is constructed in accordance with the present invention. The structure 600 comprises a first two lateral power MOSFET 102 combined with a second lateral power MOSFET 104 on a single semiconductor substrate 106. Preferably, the MOSFETs 102 and 104 have substantially similar voltage ratings

and MOSFET 104 is smaller in size than MOSFET 102. The first power MOSFET 102 functions as a power transistor and the second power MOSFET 104 functions as a sense transistor to monitor the operating conditions of the first power MOSFET 102. In one embodiment, the size of sense MOSFET 104 is substantially smaller than the size of main MOSFET 102. In another embodiment, the sense MOSFET 104 is $1/10^{th}$ the size of the main MOSFET 102. The structure 600 has five leads and includes a common source terminal 108, two electrically isolated drain terminals 109 and 110 and two electrically isolated gate terminals 112 and 113.

[0047] The source terminal of the power MOSFET 102 is connected to the source terminal of the sense MOSFET 104 to function as the common source terminal 108 of the structure 600. The drain terminal of the power MOSFET 102 functions as the isolated drain terminal 109 of the structure 600. The drain terminal of the sense MOSFET 104 functions as the isolated drain terminal 110 of the structure 600. The gate terminal of the power MOSFET 102 functions as the isolated gate terminal 112 of the structure 600. The gate terminal of the sense MOSFET 104 functions as the isolated gate terminal 113 of the structure 600.

[0048] FIG. 7 is an exemplary, physical cross-sectional diagram of a monolithic structure 601, which implements the schematic shown in FIG. 6.

[0049] FIG. 8 is a schematic diagram of an alternative embodiment of a monolithic structure 700 having an integrated drain sense that is constructed in accordance with the present invention. The structure 700 comprises at least two lateral power MOSFETs 102 and 104 of preferably equal voltage ratings which are combined on a single semiconductor substrate 106. The first power MOSFET 102 functions as a power

transistor and the second power MOSFET 104 functions as a sense transistor to monitor the operating conditions of the first power MOSFET 102. The structure 700 has four leads and includes a common source terminal 108, two electrically isolated drain terminals 109 and 110 and a common gate terminal 112/113.

[0050] The source terminal of the power MOSFET 102 is connected to the source terminal of the sense MOSFET 104 to function as the common source terminal 108 of the structure 700. The drain terminal of the power MOSFET 102 functions as the isolated drain terminal 109 of the structure 700. The drain terminal of the sense MOSFET 104 functions as the isolated drain terminal 110 of the structure 700. The gate terminal of the power MOSFET 102 is connected to the gate terminal of the sense MOSFET 104 to function as the common gate terminal 112/113 of the structure 700.

[0051] FIG. 9 is an exemplary, physical cross-sectional diagram of a monolithic structure 701, which implements the schematic shown in FIG. 8.

[0052] FIG. 10 is a schematic diagram of another alternative embodiment of a monolithic structure 800 having an integrated drain sense that is constructed in accordance with the present invention. The structure 800 comprises at least two lateral power MOSFETs 102 and 104, each having substantially different threshold voltages, which are combined on a single semiconductor substrate 106. The first power MOSFET 102 has a threshold voltage rating of 1.0V and functions as a power transistor. The second power MOSFET 104 has a threshold voltage rating of 0.5V and functions as a sense transistor to monitor the operating conditions of the power MOSFET 102. The MOSFET structure 800 has four leads and includes a common source terminal 108, two electrically isolated drain terminals 109 and 110 and a common gate terminal 112/113.

[0053] The source terminal of the power MOSFET 102 is connected to the source terminal of the sense MOSFET 104 to function as the common source terminal 108 of the structure 800. The drain terminal of the power MOSFET 102 functions as the isolated drain terminal 109 of the structure 100. The drain terminal of the sense MOSFET 104 functions as the isolated drain terminal 110 of the structure 800. The gate terminal of the power MOSFET 102 is connected to the gate terminal of the sense MOSFET 104 to function as the common gate terminal 112/113 of the structure 800.

[0054] FIG. 11 is an exemplary, physical cross-sectional diagram cross-sectional diagram of a monolithic structure 801, which implements the schematic shown in FIG. 10. Optionally, structure 801 includes an threshold adjust implant.

[0055] ADVANTAGES

[0056] The monolithic structures of the present invention provide several advantages over the prior art. First, the monolithic structures have a lower gate charge and gate resistance, similar on-resistance, less interconnect parasitics, and faster transition between the catch and forward MOSFETs than the prior art discrete circuit implementation. Second, the monolithic structures replace the two secondary-side synchronous catch and forward MOSFETs and a separate external MOSFET, thus reducing the number of device parts.. Third, the monolithic structures have a small footprint, low profile, low interconnect impedance and junction-side cooling capability. Fourth, the the monolithic structures provide improved parametric matching of both the power and sense transistors. Fifth, main and sense MOSFETs relative sizes can be accurately established thus allowing the area dependent parameters of the monolithic structure's combined (main) and sense MOSFETs to be accurately ratioed . Sixth, the monolithic structures feature

excellent temperature tracking for improved matching and accuracy. Seventh, the threshold voltages of the combined switch and sense MOSFETs of the monolithic structures can be adjusted independently for use in applications where this would be advantageous.

[0057] CONCLUSION

[0058] Having now described preferred embodiments of the invention, it should be apparent to those skilled in the art that the foregoing is illustrative only and not limiting, having been presented by way of example only. All the features disclosed in this specification (including any accompanying claims, abstract, and drawings) may be replaced by alternative features serving the same purpose, and equivalents or similar purpose, unless expressly stated otherwise. Therefore, numerous other embodiments of the modifications thereof are contemplated as falling within the scope of the present invention as defined by the appended claims and equivalents thereto.

CLAIMS

What is claimed is:

1. A monolithic structure, comprising:

a semiconductor substrate having a first surface;

one or more first lateral device having a first source terminal, a first drain terminal and a first gate terminal; said first source, drain and gate terminals terminating on said first surface;

one or more second lateral device having a second source terminal, a second drain terminal and a second gate terminal; said second source, drain and gate terminals terminating on said first surface; and;

said one or more first lateral device being combined with said one or more second lateral power transistor device on said substrate.

2. The monolithic structure of claim 1 further comprising at least one first electrically isolated lead comprising said first source terminal being connected to said second source terminal.

3. The monolithic structure of claim 2 further comprising at least one second and third electrically isolated leads comprising said first and second drain terminals; wherein said first and second drain terminals being electrically independent of each other.

4. The monolithic structure of claim 3 further comprising at least one third and fourth electrically isolated leads comprising said first and second gate terminals; wherein said first and second gate terminals being electrically independent of each other.

5. The monolithic structure of claim 3 wherein said first gate terminal being connected to said second drain terminal; said second gate terminal being connected to said first drain terminal.

6. The monolithic structure of claim 1 wherein each of said first and second lateral devices is a lateral power MOSFET.

7. A monolithic structure comprising at least two lateral power transistor devices combined on a semiconductor substrate, said structure comprising;

a semiconductor substrate having a first surface;

a first lateral power transistor device having a first source terminal, a first drain terminal and a first gate terminal; said first source, drain and gate terminals terminating on said first surface;

a second lateral power transistor device having a second source terminal, a second drain terminal and a second gate terminal; said second source, drain and gate terminals terminating on said first surface;

said first gate terminal being connected to said second drain terminal; said second gate terminal being connected to said first drain terminal; said first and second drain terminals being electrically independent of each other;

a first electrically isolated lead comprising said first source terminal being connected to said second source terminal;

a second electrically isolated lead comprising said first drain terminal; and

a third electrically isolated lead comprising said second drain terminal.

8. The monolithic structure of claim 7 wherein each of said first and second lateral power transistor devices is a lateral power MOSFET.

9. A monolithic structure comprising at least two lateral power transistor devices combined on a semiconductor substrate, said structure comprising;

a semiconductor substrate having a first surface;

a first lateral power transistor device having a first source terminal, a first drain terminal and a first gate terminal; said first source, drain and gate terminals terminating on said first surface;

a second lateral power transistor device having a second source terminal, a second drain terminal and a second gate terminal; said second source, drain and gate terminals terminating on said first surface;

said first and second drain terminal being electrically independent of each other;

a first electrically isolated lead comprising said first source terminal being connected to said second source terminal;

a second electrically isolated lead comprising said first drain terminal;

a third electrically isolated lead comprising said second drain terminal; and

a fourth electrically isolated lead comprising said first gate terminal being connected to said second gate terminal.

10. The monolithic structure of claim 9 wherein each of said first and second lateral power transistor devices is a lateral power MOSFET.

11. The monolithic structure of claim 9 wherein said second lateral power transistor is of substantially smaller size than said first lateral power transistor.

12. The monolithic structure of claim 9 wherein said first and second lateral power transistors each have substantially different threshold voltages; said difference in threshold voltages ranging from approximately 0.1V and greater.

13. A monolithic structure comprising at least two lateral power transistor devices combined on a semiconductor substrate, said structure comprising;

a semiconductor substrate having a first surface;

a first lateral power transistor device having a first source terminal, a first drain terminal and a first gate terminal; said first source, drain and gate terminals terminating on said first surface;

a second lateral power transistor device having a second source terminal, a second drain terminal and a second gate terminal; said second source, drain and gate terminals terminating on said first surface;

said first and second gate terminals being electrically independent of each other; and; said first and second drain terminal being electrically independent of each other;

a first electrically isolated lead comprising said first source terminal being connected to said second source terminal;

a second electrically isolated lead comprising said first drain terminal;

a third electrically isolated lead comprising said second drain terminal;

a fourth electrically isolated lead comprising said first gate terminal; and

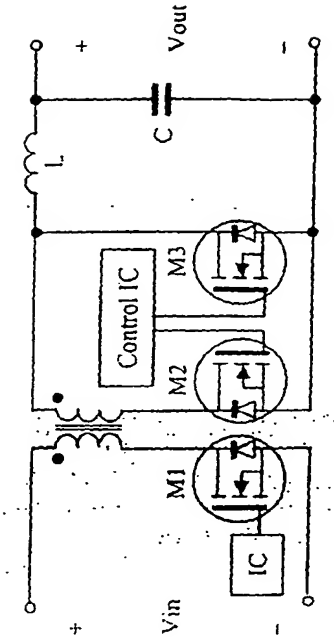
a fifth electrically isolated lead comprising said second gate terminal.

14. The monolithic structure of claim 13 wherein each of said first and second lateral power transistor devices is a lateral power MOSFET.

15. The monolithic structure of claim 13 wherein said second lateral power transistor is of substantially smaller size than said first lateral power transistor.

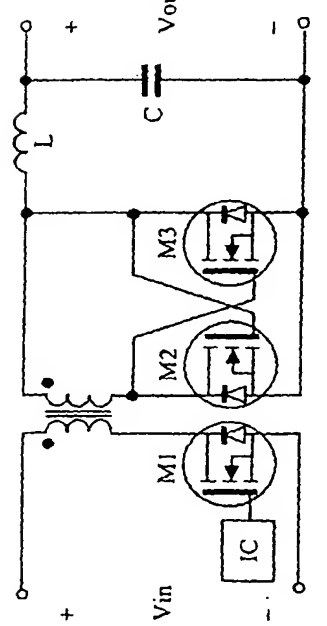
16. The monolithic structure of claim 13 wherein said first and second lateral power transistors each have substantially different threshold voltages; said difference in threshold voltages ranging from approximately 0.1V and greater.

Figure 1



IC-driven synchronous rectification isolated forward converter

1B



Self-driven synchronous rectification isolated forward converter

1A

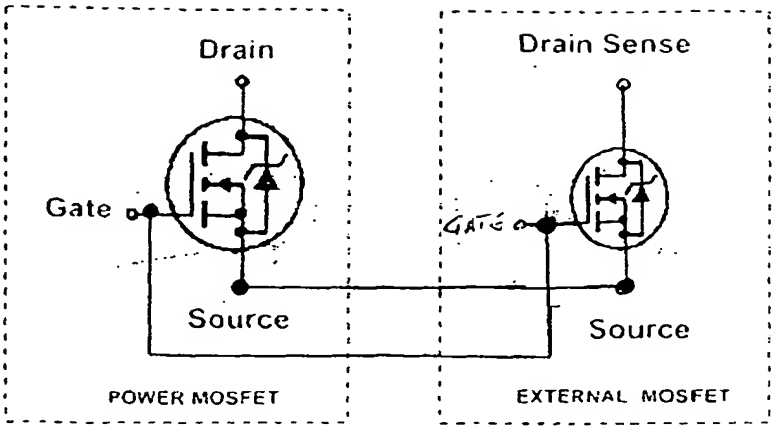
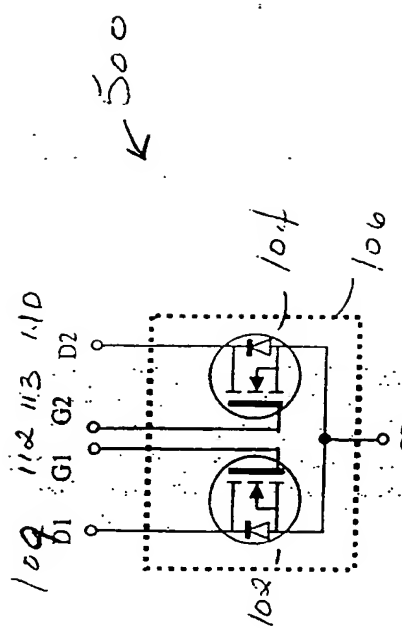
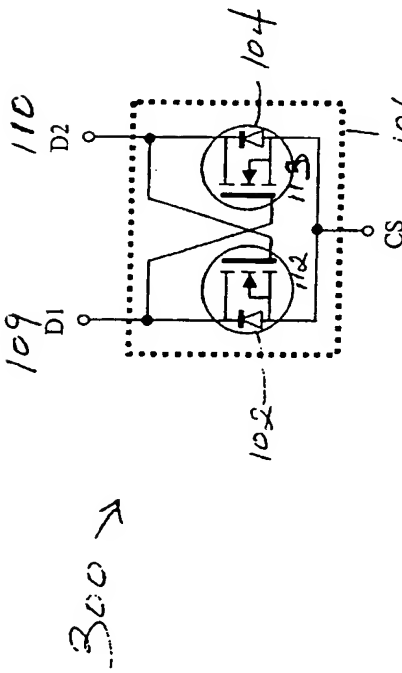

Drain
Drain Sense
Gate
GATE
Source
Source
POWER MOSFET
EXTERNAL MOSFET

FIG. 2



Second embodiment:
5-lead control IC-driven
synchronous rectification
MOSFET pair

Figure 3b



First embodiment:
3-lead self-driven
synchronous rectification
MOSFET pair

Figure 3a

Figure 3

Figure 4

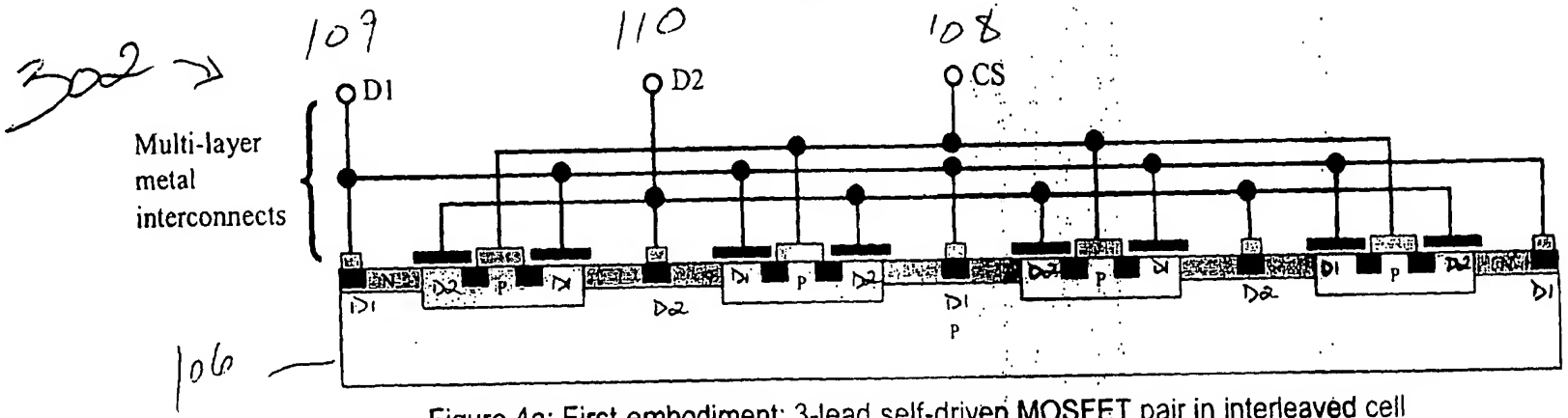


Figure 4a: First embodiment: 3-lead self-driven MOSFET pair in interleaved cell fingers

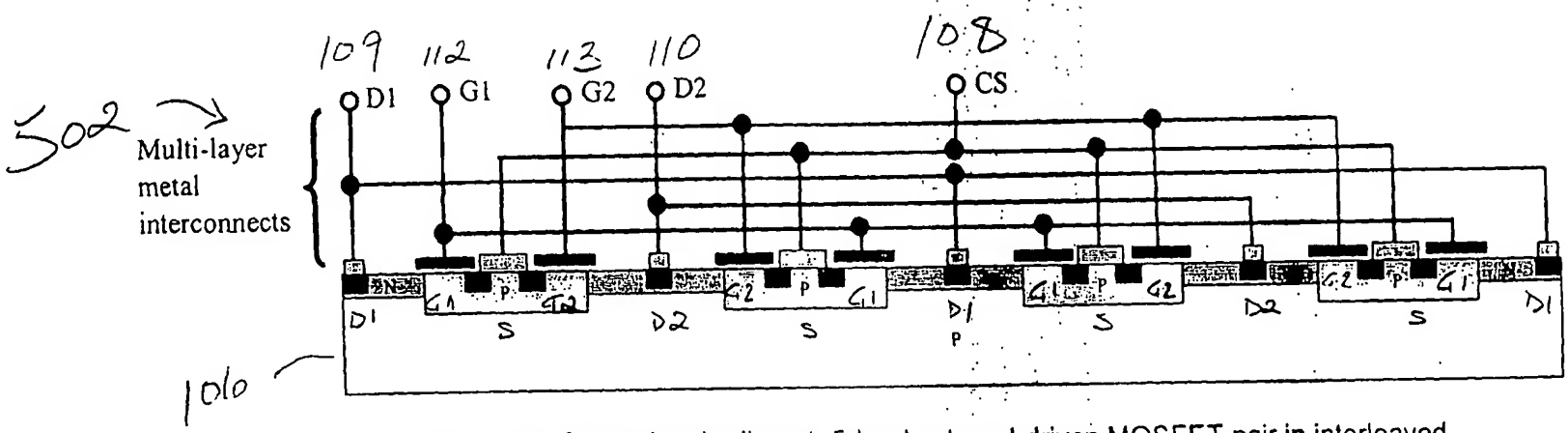


Figure 4b: Second embodiment: 5-lead external-driven MOSFET pair in interleaved cell fingers

Figure 5

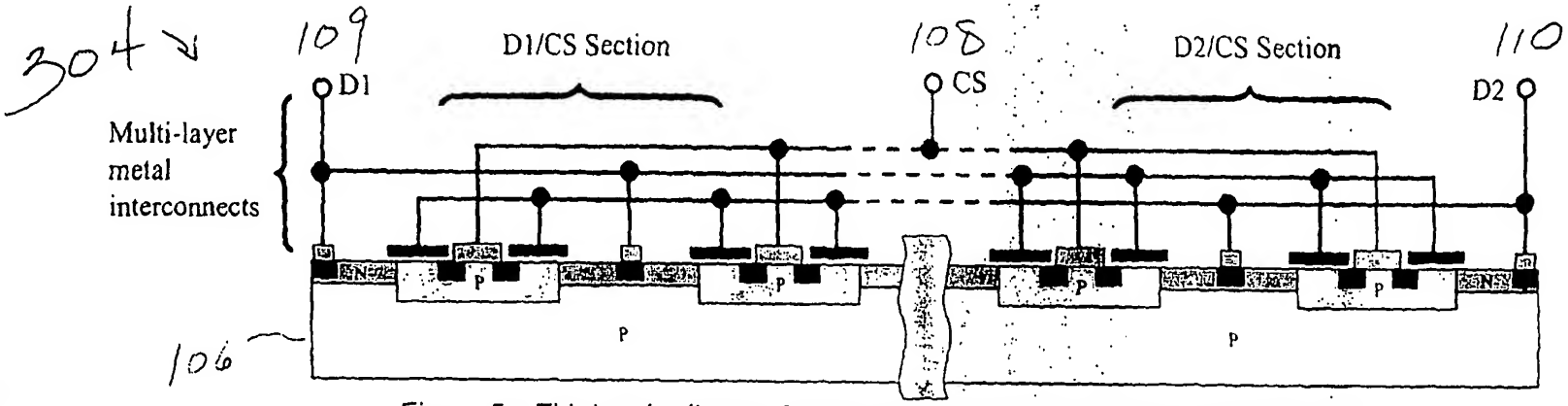


Figure 5a: Third embodiment: 3-lead self-driven MOSFET pair in separate cell sections

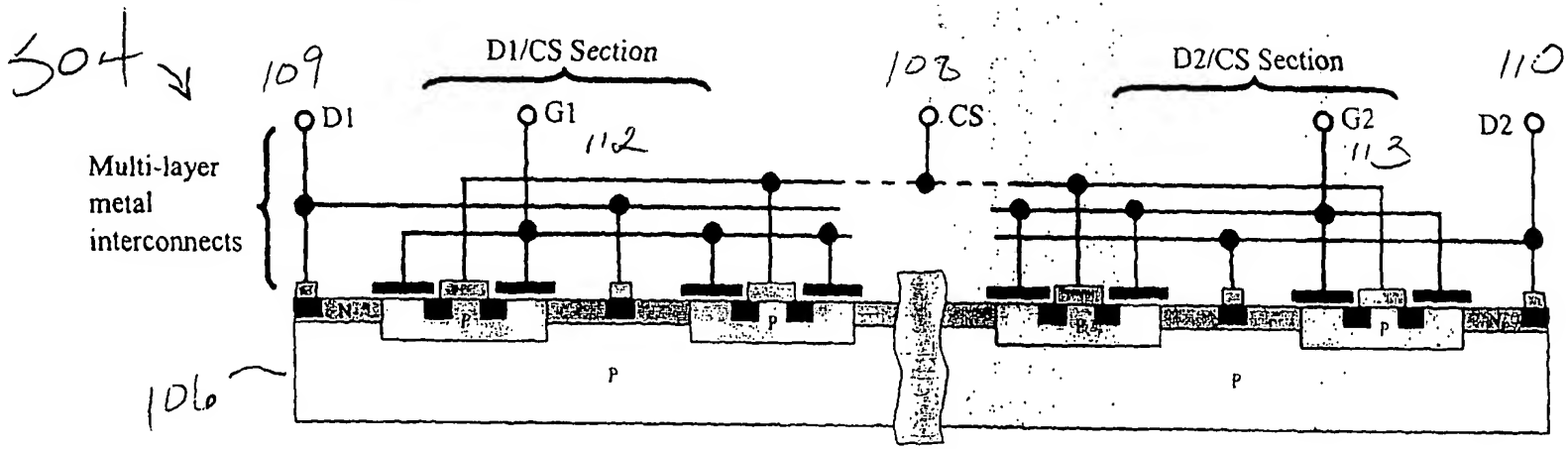


Figure 5b: Fourth embodiment: 5-lead external-driven MOSFET pair in separate cell sections

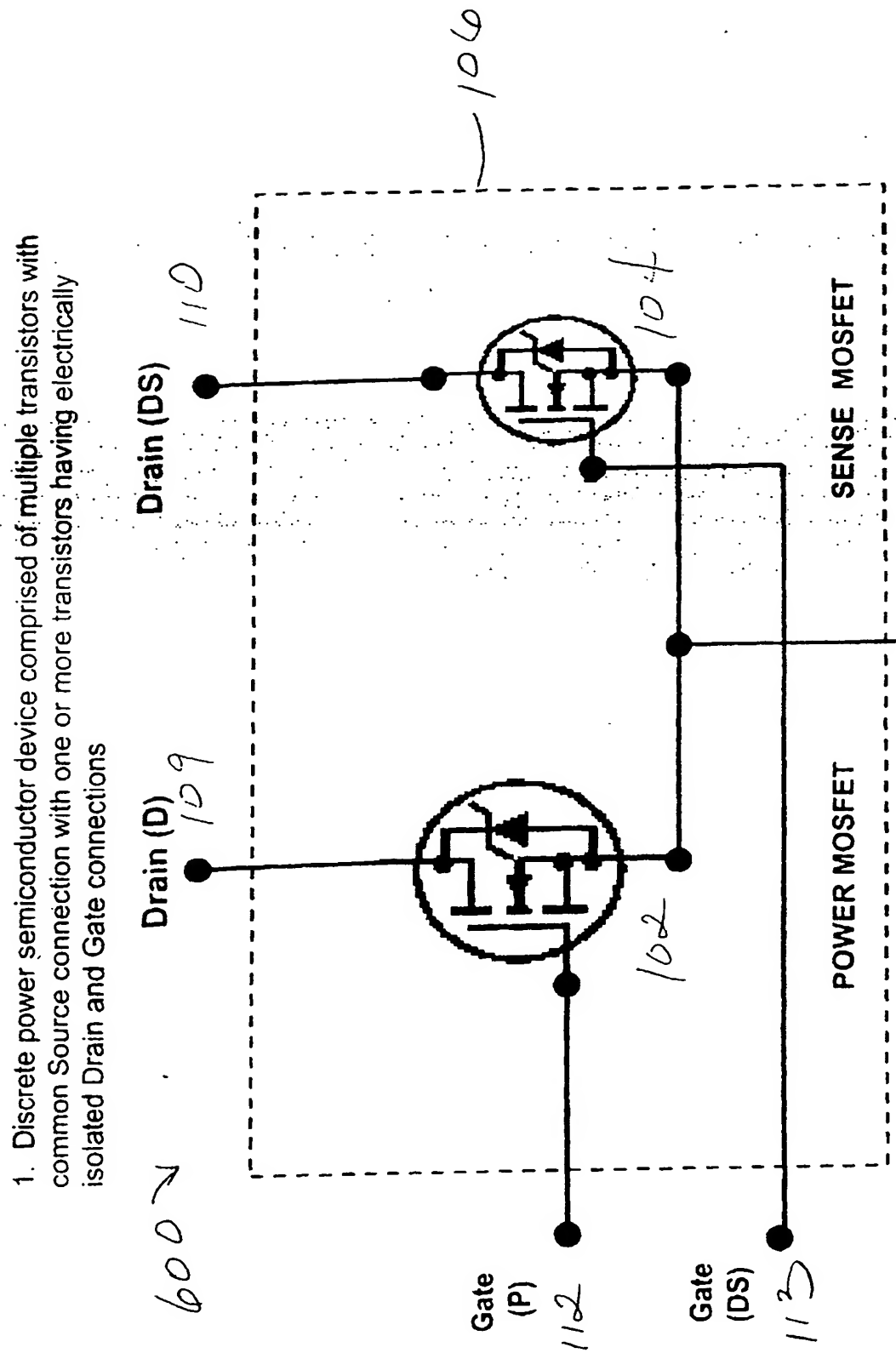


Fig 6

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1. Discrete power semiconductor device comprised of multiple transistors with common Source connection with one or more transistors having electrically isolated Drain and Gate connections

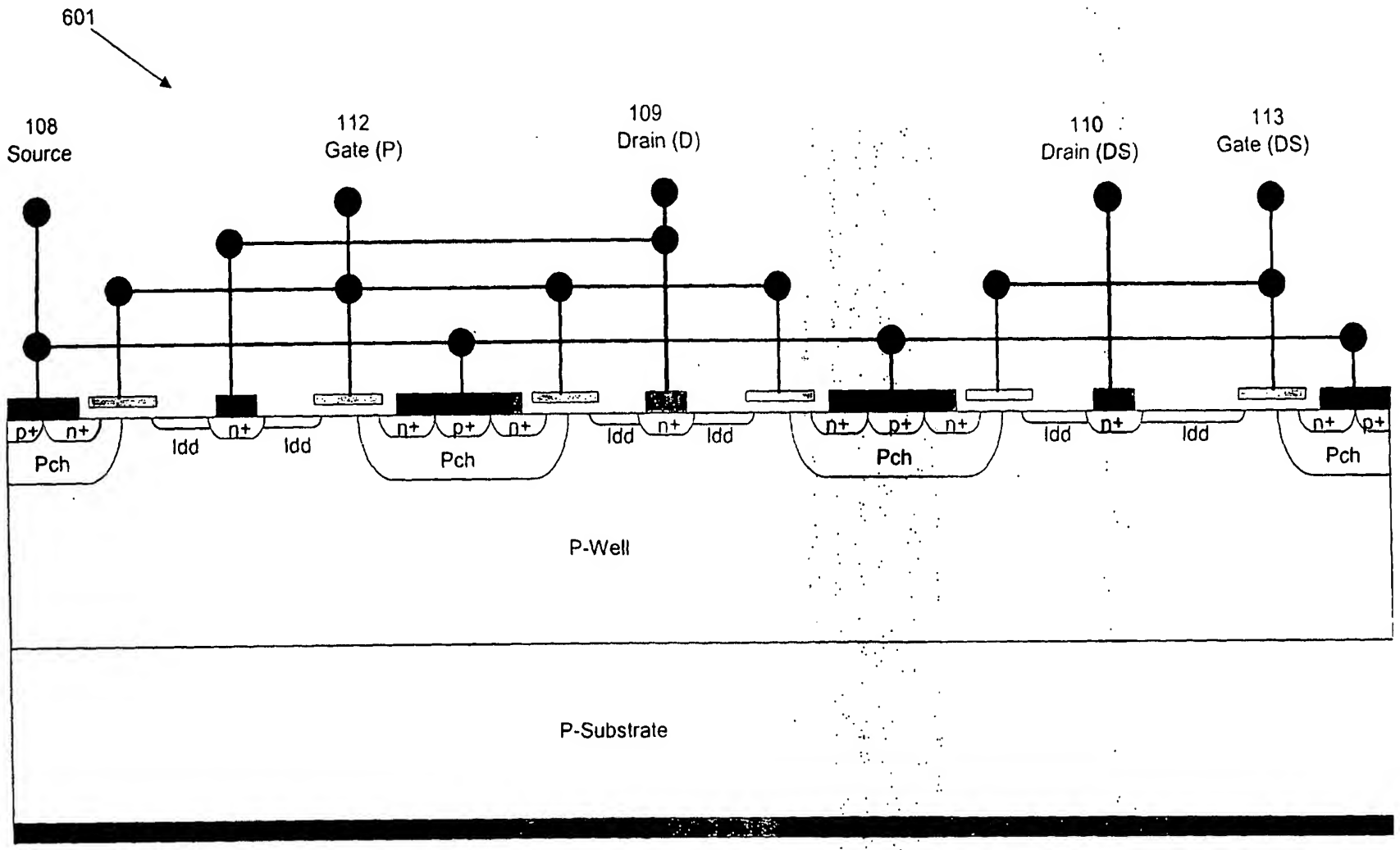

Figure 7

Cross-Sectional Diagram of a Power MOSFET With Integrated Drain Sense

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PCT/US2004/041243

2. Discrete power semiconductor device comprised of multiple transistors with common Source and Gate connections with one or more transistors having electrically isolated Drain connections

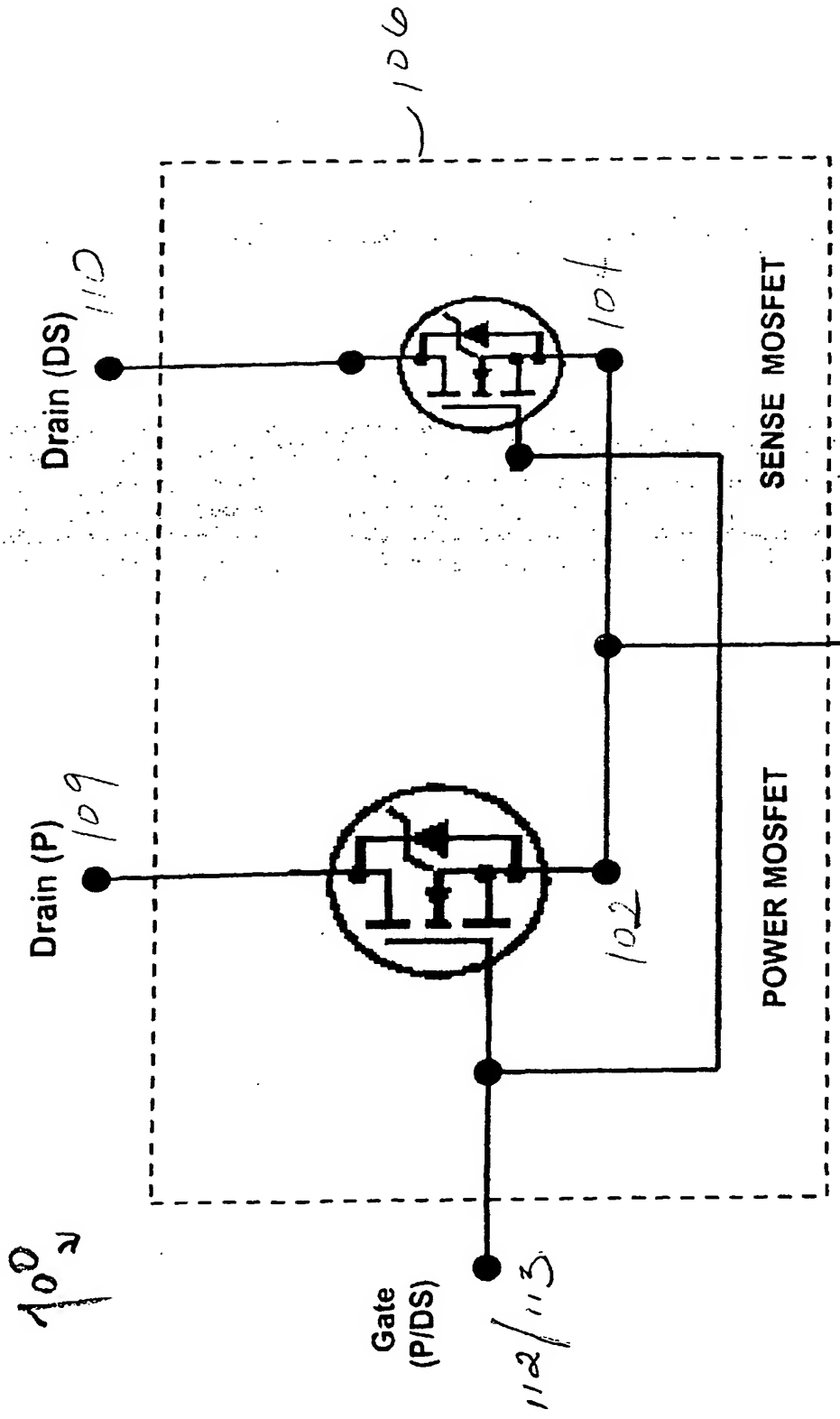

FIG 8

2. Discrete power semiconductor device comprised of multiple transistors with common Source and Gate connections with one or more transistors having electrically isolated Drain connections

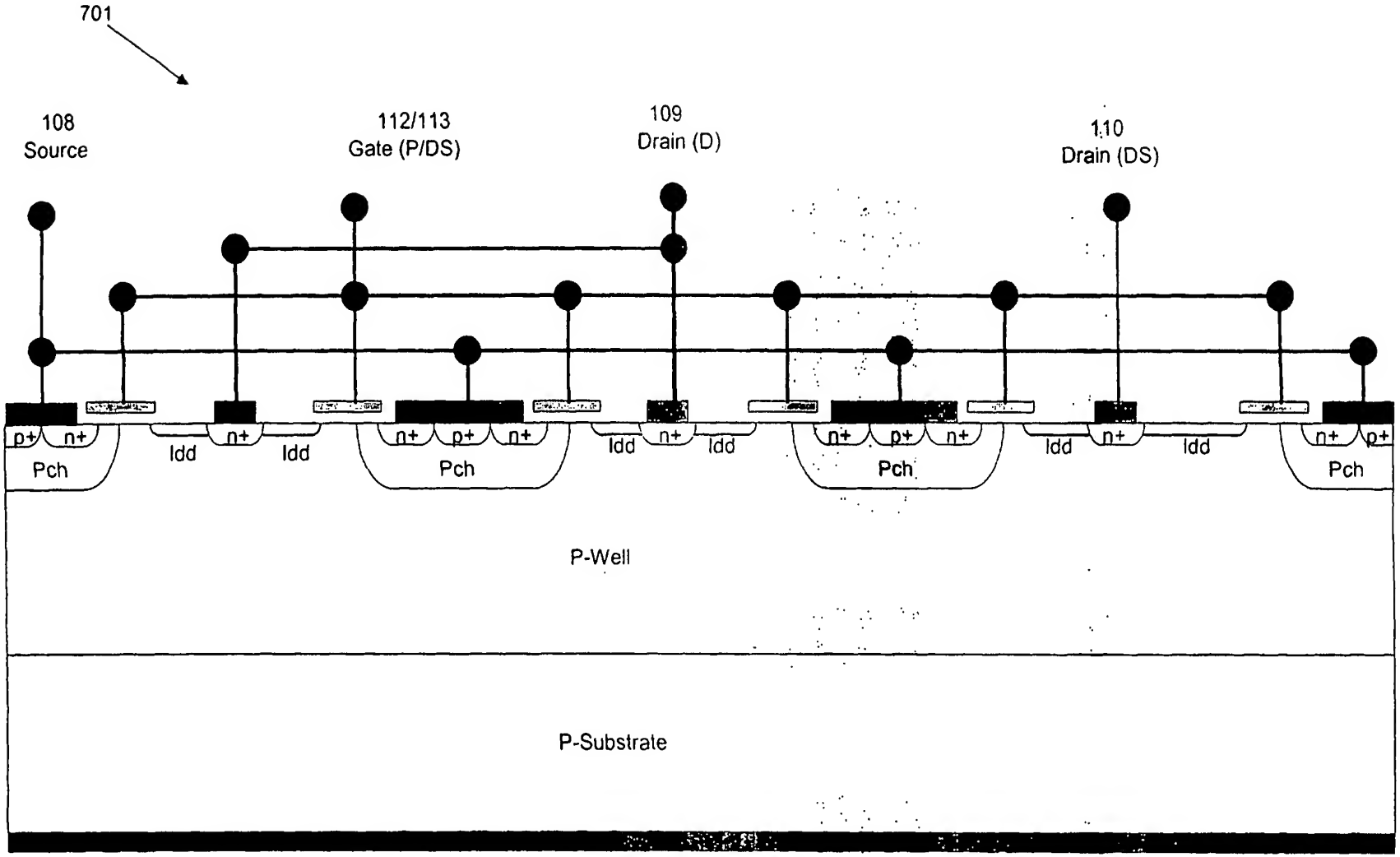

Figure 9

Cross-Sectional Diagram of a Power MOSFET With Integrated Drain Sense

3. Discrete power semiconductor device comprised of multiple transistors with common Source and Gate connections with one or more transistors having substantially different threshold voltages and electrically isolated Drain connections

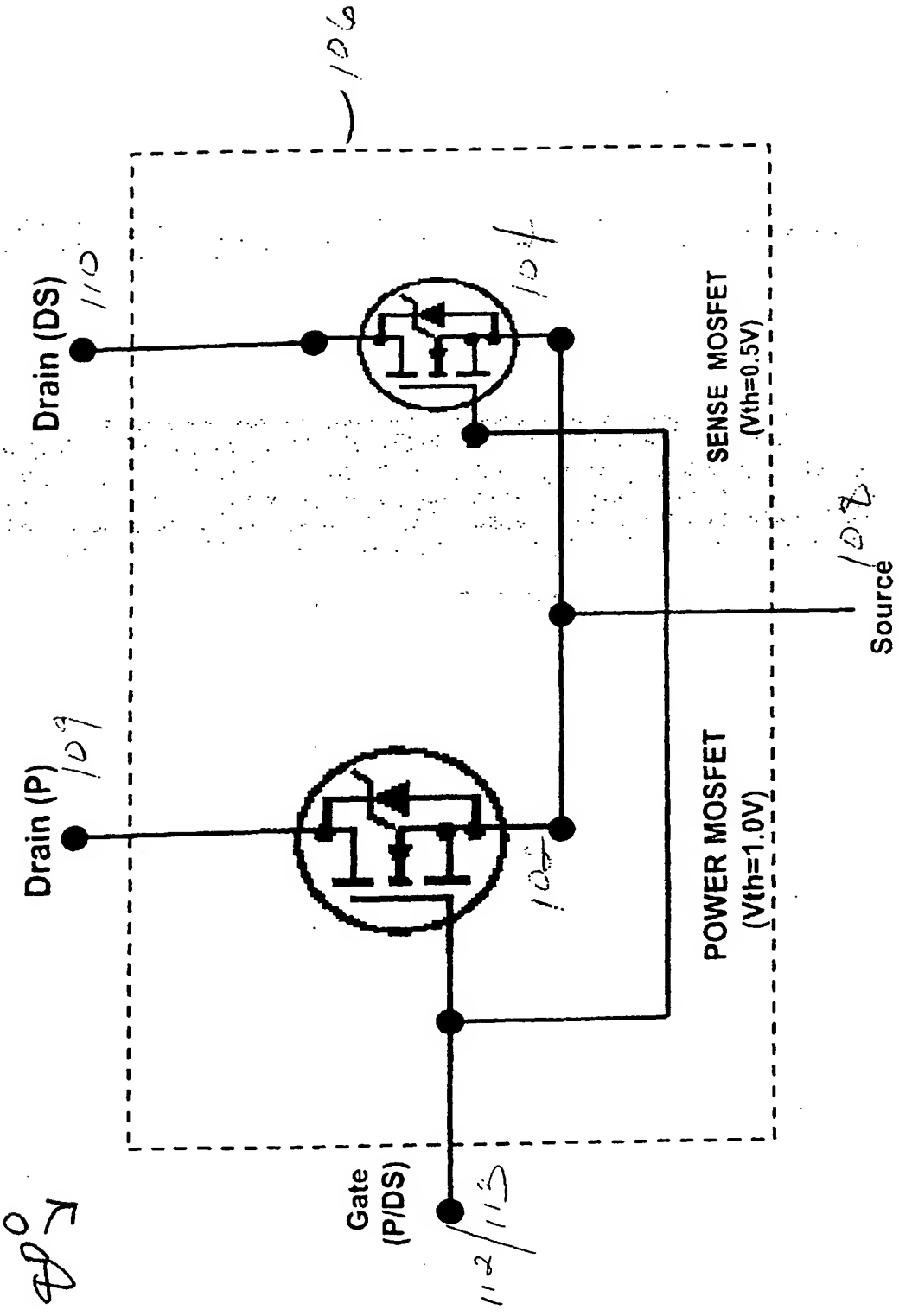

FIG. 10

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3. Discrete power semiconductor device comprised of multiple transistors with common Source and Gate connections with one or more transistors having substantially different threshold voltages and electrically isolated Drain connections

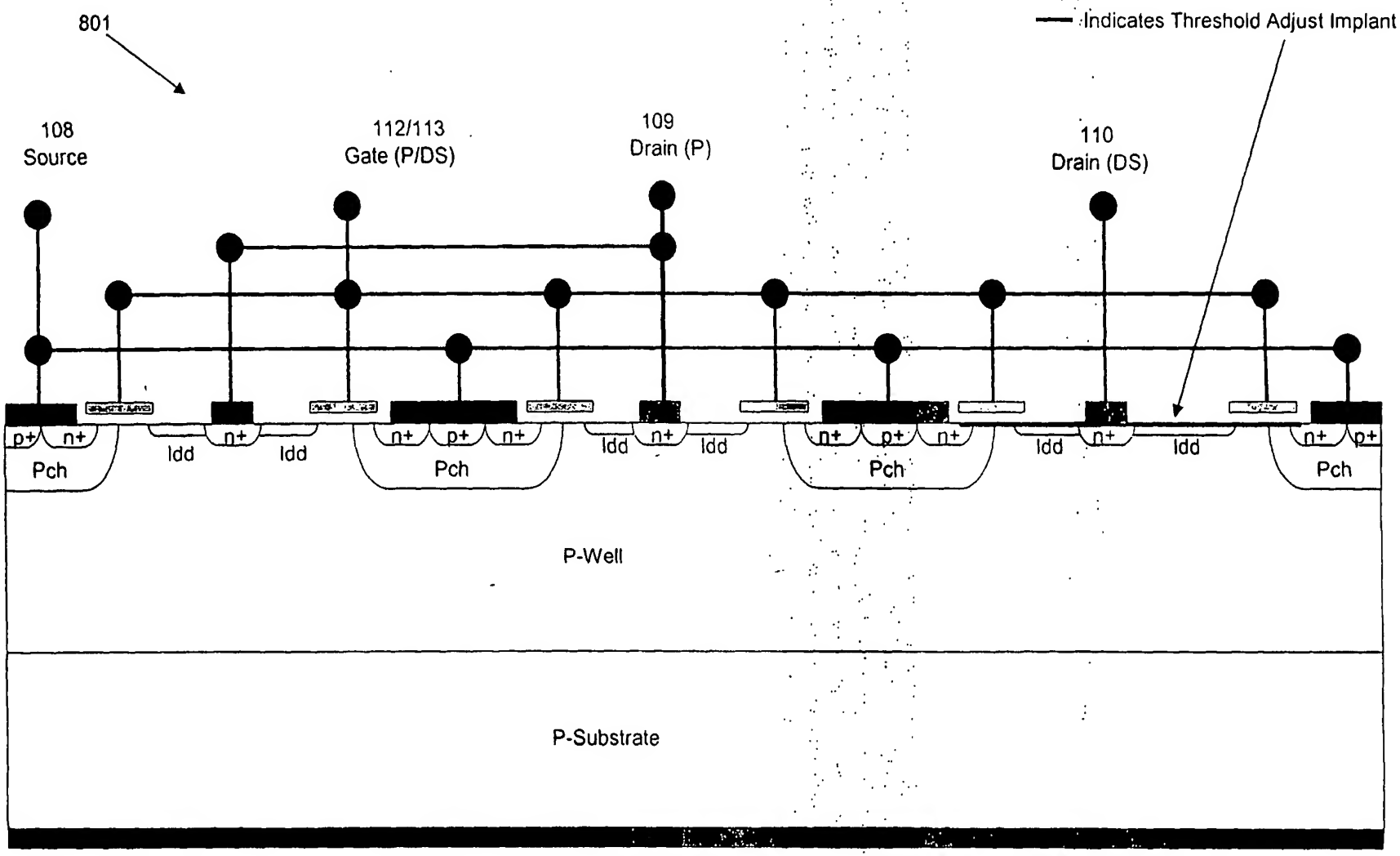

Figure 11

Cross-Sectional Diagram of a Power MOSFET With Integrated Drain Sense